Low Power Dynamic Logic Circuit Design Using Footed Diode Domino Logic

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Abstract—In recent electronic devices power saving has more importance than any other thing. Dynamic logic circuits are one of the basic power efficient circuits which come into picture when dealt with low power. Dynamic logic circuits operate mainly in two phases, namely Pre-charge and Evaluate phase. Domino logic circuits are more power efficient and cooperatively faster circuits which operate on the above two phases. For extremely low power applications footed diode domino logic is applied. This project mainly deals with design of Dynamic logic circuit design based on footed diode domino logic with reduction in power and leakage current. In this proposed circuit we put a diode on the foot of domino logic circuit which results in power reduction as compared to reported and conventional domino logic. We are using NMOS as a diode and due to this extra diode (NMOS), in pre-charge period leakage current reduce due to stacking effect. Approximately 32% of power is saved using footed diode domino logic.

Keywords: NMOS, low power, Dynamic logic circuits, Pre-charge and Evaluate phase

1. INTRODUCTION

1.1 MOTIVATION:

Low power and high speed logic design circuits continue to get more attention in consideration of product manufacturing. So now a day’s power saving has more importance than any other thing. Dynamic logic circuits came into the picture because of power efficient circuitry.

Domino logic circuits are more power efficient and cooperatively faster, so these circuits have almost half the transistor count with respect to complementary static circuits. Domino logic is basically a dynamic logic circuit followed by a static inverter and having a capacitor as a load. The clock signal is used to control the operation of domino logic circuit. The output of the dynamic logic circuit is stored in the parasitic capacitance which is located just before the static inverter. The parasitic capacitance just stores the output voltage and passes it to the next state which is the output stage of the domino circuit and stored in the load capacitor. The dynamic logic circuit requires two phases. The first phase, when Clock is low, is called

the pre-charge phase and the second phase, when Clock is high, is called the evaluation phase. In the setup phase, the output is driven high unconditionally (no matter the values of the inputs). The capacitor, which represents the load capacitance, becomes charged. Because the transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase. During the evaluation phase, Clock is high. In the pre-charge phase also extra noise is introduced to the dynamic circuit. Dynamic logic design using pseudo dynamic buffer has been done. When the circuit is in the pre-charge phase, pre-charge pulse is blocked at input of the buffer and stopped from being passed to the domino gate, and as a result power is saved during the pre-charge pulse. To reduce more power subsequently in the pre-charge phase we proposed a diode footed dynamic clock controlled circuit. Using this diode footed dynamic structure pre-charge pulse is blocked & prevented to pass through the buffer. So, during the pre-charge phase more power saved as compared. As a result our proposed circuit is more power efficient in comparison with reported and TSPC based dynamic logic design.

1.2 CONVENTIONAL DOMINO LOGIC

The schematic of a conventional footed clock controlled domino logic circuit, which consists of a dynamic N-type gate (Pull-down network PDN) followed by a static inverter. Fig. 1.1 illustrates the implementation of a domino logic buffer. The gate operates in two phases, namely pre-charge and evaluation phases. During the pre-charge phase the clock signal clk is pulled low thus turning on the PMOS transistor M1 enabling to pre-charge the dynamic node Z. During the evaluation phase, the clock signal clk is pulsed high, thus turning on the NMOS transistor M2. When the input A is low, the logic at node Z is kept high regardless of the operating phase. However, when the input A is high, two phases (evaluation and pre-charge) should be discussed as depicted in Fig.1.2.

During the pre-charge phase, node Z is charged up to Vdd as well as node B. The voltage at node F drops down to ‘0’, resulting in a propagation of the pre-charge phase to the output of the buffer. The propagation of the pre-charge pulse from node Z through the static buffer results in increased power consumption. In addition, the output logic is unstable during the pre-charge phase.
1.3 PSEUDO BASED DOMINO LOGIC

The previous section illustrates the issue of performance degradation due to the propagation of the pre-charge pulse inherent in domino logic gates. The proposed PDB-based implementation overcomes this problem using the circuit structure shown in Fig 1.3. In the proposed implementation of the buffer, the source of the buffer’s NMOS transistor M5 is connected to node B instead of Gnd. Using the propagation of the pre-charge pulse from node Z through the static buffer results in increased power consumption. In addition, the output logic is unstable during the pre-charge phase and as a result, the cascading performance is limited such a circuit topology, the value at node Z cannot propagate to the output F during the pre-charge phase of the gate since during this phase, the evaluation transistor M2 is turned off. For our proposed gate, when the input logic A is low, the floating node Z is always high and then, the output node F is kept low regardless of the operating phase. On the other hand, if the input A is high, the pre-charge and evaluation phases will lead to the following situation.

During the evaluation phase, node Z is discharged to Gnd as well as node B, resulting in enabling the PMOS transistor M4, while pulling up the output F to Vdd. During the pre-charge phase node Z is charged up to Vdd, followed by the voltage at node B. Since the NMOS evaluation transistor M2 is disabled the output node Z is held high. It is important to note that during the pre-charge phase, the output node F is isolated from Gnd. In other words, the pre-charge pulse at node Z cannot propagate through the buffer to the output node F.

1.3.1 POWER ANALYSIS OF PSEUDO BASED DOMINO LOGIC:

In the proposed domino logic, the pre-charge pulse is prevented from propagating to the output node of the buffer, resulting in a decreasing current consumption in the output stage of the domino gate. Ideally, if the pre-charge pulse propagating is completely prevented and the input logic is fixed to ‘1’, the power saving Z of the proposed scheme compared to conventional domino logic can be approximately given as:

\[
\text{Power saving } Z = \frac{\text{Power consumption of conventional domino logic} - \text{Power consumption of proposed PDB domino logic}}{\text{Power consumption of conventional domino logic}} \times 100 \%
\]

The power saving of the proposed scheme comes from reducing the output node activity. Typically there are three limits which can degrade the power saving. The first one is the logic activity rate. The power saving is maximized when it is fixed to ‘1’, because the output node F is also fixed to ‘1’ and...
capacitors Cbuf and Cload are not b
e charged .When the logic
activity is increased, the output stage consumes more power and
as a result, the power saving of the proposed scheme is reduced.
The second non-ideal restriction is due to the internal capacitance CB.

In the conventional scheme, the NMOS transistors
source of the output stage is always connected to ground.
Therefore, the parasitic capacitor in this source node does not
consume power. However, in the proposed domino scheme, the
capacitance of node B consists of the parasitic capacitors of both
the first stage NMOS transistors and the output stage NMOS
transistor .As a result, the cap load in the proposed scheme is
increased leading to a larger power consumption. The third limit
is the charge sharing, which is mainly generated due to a finite
clock slew rate. During the clock transition from ‘1’ to ‘0’, the
time at node B will be charged from both node Z and node F,
leading to a output charge sharing. As discussed above, when
comparing with the conventional domino logic, the power saving
by using the proposed scheme is coming from the reduced
activity of the buffer output.

1.4 FOOTED DIODE DOMINO LOGIC

Performance degraded in a circuit is due to propagation
of pre-charge pulse from dynamic node to the output node. The
PDB based design for domino logic compensates this problem
up to some extent but there is always a room for improvement.
In our proposed circuit we put an NMOS transistor which is
working as a diode in between GND and M2 clock transistor.
Let us take an example of a diode footed buffer shown in the fig.
1.5. The source of the NMOS transistor m5 is connected to the
node B instead of the GND. An NMOS transistor is introduced
in the circuit whose gate is shorted with its drain and connected
to the source of the NMOS clock transistor M2, the source of
NMOS transistor M6 is connected to ground. In the circuit when
input A is low then dynamic node Z is always high and output is
kept low regardless of operating phase.

When input A is high then circuit will efficiently
operate under two phases namely pre-charge and evaluation

is turned on so, the dynamic node Z discharges through node B
and therefore output node became high.

Pre-charge phase- in this phase when clock pulse is
kept low then pmos clock transistor M5 is turned on and
dynamic node Z is charged to VDD. The output is still high
because the clock pulse turns off the transistor M2 so, M6 is also
off and therefore output node is not able to discharge. Due to
stacking effect power is compensated.

II. LITERATURE SURVEY

Literature survey

- DYNAMIC LOGIC

1. Jan M. Rabe, Anantha Chandrakasan, Borivoje
Nikolic, Digital Integrated Circuits- A Design Perspective,

Dynamic logic is normally done with capacitive charging and
discharging. The voltage at the output of the dynamic circuit is
stored on a parasitic capacitance, which is typically buffered
before it is sent to the next stage. This temporary voltage is
affected not only by charge sharing of the internal parasitic
capacitances but also by the consequent dynamic circuit.

2. A.k. Pandey, R.A. Mishra, R.K. Nagaria, Low power
dynamic buffer circuit, VLSICS, Vol.3, No.5, Oct.20
Pg.53-65

Domino logic circuits are used in wide applications such as
microprocessor memory digital logic etc. It has superior
advantage over static logic circuit, it require less number of
transistor count and reduces output load capacitance hence
enhance the speed. Realization of wide fan-in OR gate using
static logic circuit requires long stack of PMOS which is not
practical, it increase the delay and area. But domino logic use
dual phase namely pre-charge and evaluation to implement
complex circuit with single evaluation network. Domino circuit
has drawback of high power consumption due to clock loading
and reduce noise margin due to charge sharing and charge
leakage. Charge sharing is compensated by adding keeper
transistor.

3. Yolin Lih, Nestoras Tzartzanis, William W. Walker, A
leakage current

Fig 1.5: Footed diode domino logic
Evaluation phase- in this phase when clock pulse is kept high
then the PMOS transistor MI is turned off and NMOS transistor

Fig 1.5: Footed diode domino logic
When scaling down into deep sub micron technology leakage is a main problem. In this paper, new simulation and statically leakage current estimation methods are mentioned. Average leakage current macro model is introduced.


As a result of the continuously increasing complexity of integrated circuits, it is very important to use simplified design methods in order to limit the design time. This is also true for the timing part of the design, where a general and safe clocking principle should be used. The most popular principle of this type is the two-phase non-overlapping clock. In CMOS this principle unfortunately expands into pseudo-two-phase clocking, really using four clock phases. It therefore needs quite a lot of silicon area for clock lines.

III. FULL ADDER

3.1 8T FULL ADDER

Here we had a full adder designed using 8 transistors.

![Fig 3.1: 8T full adder](image)

Here this full adder is designed using gate diffusion input method. The GDI methodology has originally been introduced for the design of low-power combinational synchronous circuits. We are giving input not only at gate terminal but also at source terminal.

<table>
<thead>
<tr>
<th>Average power</th>
<th>2.11814e-004 watts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum power</td>
<td>1.786513e-003 watts</td>
</tr>
<tr>
<td>Minimum power</td>
<td>8.570999e-010 watts</td>
</tr>
</tbody>
</table>

Table1: Full adder power values

3.2 PSEUDO DYNAMIC FULL ADDER CIRCUIT:

Here the source of one NMOS transistor is connected to drain of another NMOS transistor.

![Fig 3.2: Pseudo dynamic full adder circuit](image)

POWER RESULTS

v5 from time 0 to 1e-005

Table2: Pseudo dynamic full adder results

3.3 FOOTED DIODE FULL ADDER CIRCUIT

![Fig 3.3: Footed diode full adder circuit](image)

Here we are adding an additional NMOS transistor. Here Gate and drain terminal are shorted together and it acts like a diode. Stacking effect Phenomenon is applied here.

3.3.1 STACKING EFFECT

In particular serially connected devices or stacked devices have lower leakage than the sum of the leakages of all devices consumed individually. An informal definition of stack effect is: the total leakage current of cascaded transistor chain decreases with the number of stacked transistors increasing, and it is often used to reduce leakage power.

Stack effect is not only a phenomenon of transistors, but also that of whole circuits. The sub threshold leakage current flowing through a stack of transistors connected in series is reduced if at least one of them is switched off.

To demonstrate the stack effect of transistors we have to conduct experiments to calculate the total leakage currents for different number of cascaded PMOS and NMOS transistors with high and low threshold voltages.
IV. RIPPLE CARRY ADDER:

4.1 RIPPLE CARRY ADDER:

Fig 4.1: Ripple carry adder

4.1.1 DESIGNED RIPPLE CARRY ADDER CIRCUIT:

Fig 4.2: Ripple carry adder circuit diagram

DOMINO RIPPLE CARRY ADDER

Fig 4.3: Domino ripple carry adder

4.3 FOOTED DIODE DOMINO RIPPLE CARRY ADDER

CONCLUSION

Due to propagation of the pre-charge pulse to the output node in conventional domino logic increased the power dissipation by the circuit. The prorogation of pre-charge pulse to output node is prevented by using pseudo domino logic and some power has been saved. This project proposes a footed diode domino logic style design which can reduce leakage current and more power has been saved as compared to other logic style. Approximately 32% of power is saved using footed diode domino logic compared to pseudo domino logic.

BIBILOGRAPHY


