

# A New Compensation Technique for Stable The Gain of Sub-Micron Amplifiers

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**Abstract**—Process variation is an difficulty in designing reliable CMOS mixed signal systems with high yield. To minimize the variation in voltage gain due to variations in process, supply voltage, and temperature for common trans conductance-based amplifiers, we present a new compensation method based on statistical feedback of process information. We further apply our scheme to two well known amplifier topologies in the sub-micron CMOS process as design examples—an inductively degenerated low-noise amplifier (LNA) and a common source amplifier (CSA). The proposed method improves the variation in S21 of an inductively degenerated cascade LNA from 8.75% to 1.27%, which is a reduction in variation of 85%. The presented scheme is also robust over variations in supply voltage, temperature, and process conditions. The compensation method presented can be utilized to stabilize the gain of a wide variety of amplifiers.

**Index Terms**—CMOS analog integrated circuits, process compensation, process variation, self-biasing.

## INTRODUCTION

Low noise amplifiers (LNA) are the first active block in the receiver chain in RF communication systems. They are characterized by their high gain to suppress the influence of noise, their low noise figure, their 50  $\Omega$  match to both the input and output, and their linearity [1]. Advances made in CMOS have made it possible to easily integrate radio frequency communication systems on chip. However, with continuous scaling of transistor sizes to improve the performance of digital systems, RF systems have, in most cases, suffered due to increased device variability in the manufacturing process. As technologies keep scaling, accurately modeling transistor performance becomes increasingly difficult [2]. Statistical uncertainty arising from sub-wavelength lithography, diffusion process, and uneven oxide thickness translate to variations in electrical parameters such as gate length, sheet resistance, threshold voltage, and gate capacitance. Non uniform deposition and diffusion of impurities translate to variations in threshold voltage [3] [4]. Work presented in [5] shows how imperative it is to keep the power gain (S21) of the LNA stable to maintain both sensitivity effects and intermediation specifications. In this paper we determine that the variation in threshold voltage of the input transistor is the main contributor to gain variations of standard amplifier configurations where

trans conductance determines gain. With this in mind, we design and develop a compensation scheme that measures the changes in threshold voltage and generates a bias signal for amplifiers in order to minimize deviations in their voltage gain. Our scheme can be adapted to a variety of such amplifier topologies and we experimentally demonstrate the validity of our method on two well-known amplifier topologies—an inductively degenerated cascode LNA and a common source amplifier, both used as standard gain cells in many mixed-signal system applications. Both topologies have been designed in the TSMC 65 nm CMOS process.

This work presents a compensation scheme to reduce the variations in S21 of an LNA by 85%. We first identify the electrical parameters which are susceptible to variability in the manufacturing process and how they translate to variations in S21. We then propose a novel bias scheme to improve yield of LNAs and conclude with simulation results.

In Section II we introduce the related work on sub-micron amplifier compensation. We discuss Variation in the cascade LNA in section III. Design methodology in section IV. Design of bias circuit in section V. simulation results are shown in section VI. This paper concluded in section VII.

## II. RELATED WORK

Traditional approaches to detecting and correcting for variations in the gain of amplifiers have relied on using either built-in-self-test (BIST) devices, which either map the peak output signal to a corresponding DC value or introducing additional circuitry which adapts to variations in process. A survey of the state of the art of other LNA compensation schemes in literature shows good examples of these approaches.

While BIST-based methods can have precise correction, they generally require very high power back-end calibration circuitry, can affect the performance of the amplifier, and are costly in area. Han *et al.* [4] devised a calibration scheme which demonstrates significant reduction in variation of LNA gain but the presence of a DSP and tuning control circuitry makes it very costly in power and area. Jayaraman *et al.* [5] also used peak detectors to maximize S21 gain but off-chip calibration makes it impractical for onchip, low-power solutions. Sen *et al.* [6] used a sensing transistor at the output to control the current in the LNA. However, the large

transistor used in the design makes the scheme unsuitable for low supply voltage processes. Sivonen *et al.* [7] identified that the variation in gain of an LNA is a function of its load impedance and, by replacing the load resistor with a parallel combination of different resistance ratios, they demonstrated simulated voltage gain stability over process corners. However, variation of passive elements is reported to be much smaller than that of active elements [8], therefore the major contributor is the variation of the transconductance of the system. Gomez *et al.* [9] employ a biasing circuit to control the variation in the gain of LNAs, but optimally sizing the circuit trades off performance in the presence of both process and temperature variations. This causes the scheme to under-perform with PVT variations. The bias circuit also suffers from stability issues addressed in [10]. Despite the existence of various proposed schemes mentioned above, there has been no experimental demonstration as yet of a precise, low power scheme, which corrects for variations in gain of common amplifier topologies.

Our method is based on statistical feedback, where we rely on local match between transistors to track changes in threshold voltage—then generate a correction signal to feedback to the amplifier and correct for changes in gain, without affecting its operation under nominal conditions. Our method also detects and compensates for gain variations caused due to fluctuations in supply voltage. We show that our scheme can be applied to a wide variety of amplifiers, can easily be scaled for advanced CMOS processes, requiring minimal area and power overhead for its implementation. Occurring due to process and temperature variation from its nominal value. We then generate a correction signal to feed back to the amplifier and correct for changes in gain, without affecting its operation under nominal conditions. Our method also detects and compensates for gain variations caused due to fluctuations in supply voltage. We show that our scheme can be applied to a wide variety of amplifiers, can easily be scaled for advanced CMOS processes, requiring minimal area and power overhead for its implementation.

### VARIATIONS IN THE CASCODE LNA

The topology of the inductively degenerated cascode LNA, shown in Fig. 1, is chosen because it is among the most prevalent LNA architectures due to its good input power match and excellent noise performance [11] [12]. The input LC tank assists in boosting the transconductance of the input transistor and, hence, S21 of the LNA. Furthermore, the cascode configuration provides good isolation.

At the resonance frequency

$$\omega_o = \left( \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} \right)$$

Of the series RLC tank, the total transconductance of the LNA is

$$G_m = g_m Q_m = \frac{g_m}{\omega_o C_{gs} (R_s + \omega_T L_s)} \quad \text{----- (1)}$$

where gm is the transconductance of the input transistor, Cgs is its gate source capacitance, Rs is the resistance of the input source,  $\omega_T = 2\pi f$  of the input transistor, Lg is the gate inductance and LS is the value of the source degeneration inductance. To achieve zero variations in S21 of the LNA, we must eliminate variations in total transconductance. In other words, we want  $\Delta G_m = 0$ . To do this, we must understand the sources of variation in Gm by taking partial derivatives of

$$\begin{aligned} \frac{\partial G_m}{\partial g_m} &= \frac{1}{\omega_o C_{gs} (R_s + \omega_T L_s)} = \frac{G_m}{g_m} \\ \frac{\partial G_m}{\partial C_{gs}} &= \frac{-g_m}{\omega_o C_{gs}^2 (R_s + \omega_T L_s)} = \frac{-G_m}{C_{gs}} \quad \text{----- (2)} \\ \frac{\partial G_m}{\partial \omega_o} &= \frac{-g_m}{\omega_o^2 C_{gs} (R_s + \omega_T L_s)} = \frac{-G_m}{\omega_o} \end{aligned}$$

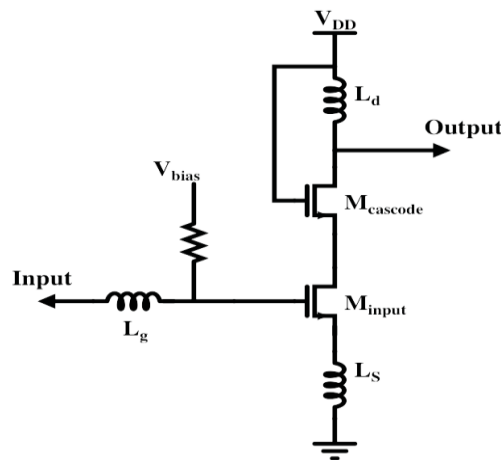


Fig1: Cascade low noise amplifier

Total variations in transconductance

$$\Delta G_m = G_m \left[ \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} - \frac{\Delta \omega_o}{\omega_o} \right] + \frac{\partial G_m}{\partial \omega_T} \Delta \omega_T$$

Since inductors can be implemented as off-chip components we can assume that they have insignificant variation in this case. Therefore

$$\frac{\Delta \omega_o}{\omega_o} = \frac{-1}{2} \frac{\Delta C_{gs}}{C_{gs}} \quad \text{----- (3)}$$

And since

$$\omega_T = \frac{g_m}{C_{gs}}$$

$$\frac{\partial G_m}{\partial \omega_T} = \frac{-G_m (L_s \omega_T)}{(R_s + \omega_T L_s)} \left( \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} \right) \quad \text{----- (4)}$$

Around the input match condition,  $R_s = \omega_T L_s$  for optimal power match. Therefore in (3)

$$\Delta G_m = G_m \left[ \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} - \frac{\Delta \omega_b}{\omega_b} - \frac{L_s \omega_T}{(R_s + \omega_T L_s)} \left( \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} \right) \right] \text{----- (5)}$$

indicates that, in order to achieve zero variation for  $G_m$  and, hence,  $S_{21}$ , the variations in output transconductance of the input transistor of the LNA must be eliminated.

$$\frac{\Delta G_m}{G_m} = \left[ \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{2C_{gs}} - \frac{1}{2} \left( \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} \right) \right] \text{----- (6)}$$

$$\therefore \frac{\Delta G_m}{G_m} = \frac{1}{2} \frac{\Delta g_m}{g_m}$$

### III. DESIGN METHODOLOGY

Similar to the methodology described in [13] for current generators, we develop an input transistor for the LNA whose output transconductance  $g_m$  total is the sum of the transconductance of two transistors  $M_1$  and  $M_2$  which are in parallel. To eliminate the variation in  $S_{21}$  of an LNA, the variation in the output transconductance of its input transistor should be zero. In our case,  $G_m$  total=0. Let us assume that  $V_{gs1}$  is set and does not vary and the nominal value of  $V_{gs2}$  is set at  $V_{gs1}$ . Transistors  $M_1$  and  $M_2$  are sized the same ( $\kappa_1=\kappa_2$ ) and placed close to each other in layout so that local match would ensure that  $V_{th1}$  approximately equals  $V_{th2}$ .

With these assumptions:

$$\begin{aligned} \Delta g_{m1} &= -2\kappa(\Delta V_{th}) + 2\Delta\kappa(V_{gs1} - V_{th}) \\ \Delta g_{m2} &= 2\kappa(\Delta V_{gs2} - \Delta V_{th}) + 2\Delta\kappa(V_{gs2} - V_{th}) \end{aligned} \text{-----(7)}$$

The variation in transconductance of the modified LNA is

$$\begin{aligned} \Delta g_{mtotal} &= \Delta g_{m1} + \Delta g_{m2} \\ \Delta g_{mtotal} &= 2\Delta g_{m1} + 2\kappa\Delta V_{gs2} \end{aligned} \text{----- (8)}$$

With no variations in transconductance of the input transistor,  $\Delta g_{mtotal}$  equals zero, and that gives

$$\Delta V_{gs2} = 2\Delta V_{th} + \frac{2\Delta\kappa(V_{gs1} - V_{th})}{\kappa} \text{----- (9)}$$

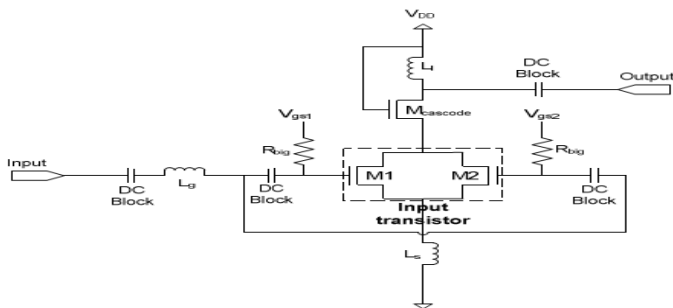


Fig2: modified LNA used as part of the schematic digram

For a cascode LNA, the input transistor would be large to achieve substantial gain; therefore  $\kappa$  for both  $M_1$  and  $M_2$  will be large. Also, for low power operation of the LNA, the input

transistor would be biased at moderate inversion to limit the current. These two assumptions allow us to conclude that the first term dominates over the second in (9) and the condition of zero variation can be approximated by

$$V_{gs2} = 2V_t \text{----- (10)}$$

gives us information about the condition for  $\Delta g_{mtotal}=0$  and it also gives us a clue to its implementation. By designing a bias circuit for transistor  $M_2$  which is able to provide the following:

$$V_{gs2} = V_{gs1} + 2V_{th} \text{----- (11)}$$

we will be able to design an LNA which has an  $S_{21}$  robust to process, supply, and temperature variations

### IV. DESIGN OF BIAS CIRCUIT

This section describes the design and implementation of a bias circuit for transistor  $M_2$  which satisfies (11). The output of this block must provide a DC bias which has an average value of  $V_{gs1}$ . It must also exhibit positive correlation with the threshold voltage by changing with twice the change in threshold voltage according to (11). by changing with twice the change in threshold voltage according to (11). variations in supply voltage. The bias circuit is designed as a four stage cascade as shown in Fig. 3. All transistors are kept in saturation and each stage is carefully sized to ensure that the condition in (11) is met for  $V_{out}$  of the bias circuit.

In the circuit,  $k_i = 1/2 \mu C_{ox}(W_i/L_i)$  for transistor  $M_1$ .  $\alpha$  is a scaling factor used to bias the NMOS transistor and is generated by using a resistive divider between  $V_{DD}$  and ground. Using wide and well matched resistors ensures that the variation on  $\alpha$  is low.  $A_i$  are relative scaling ratios for transistors in stage  $i$ . By placing the transistors close together in layout, local match is assumed and threshold variations of all transistors will be correlated. The first stage is self biased with two diode connected NMOS transistors. Subsequent stages take input only signals from the previous stage as input. The motivation for this is that the bias circuit should be self sufficient in tracking changes in threshold voltage, independent of the operation of the LNA. Analysis for each stage is provided in the remainder of this section.

#### A. First Stage:

The output signals for each stage are determined by doing a KCL analysis at each output node. Applying KCL analysis at node  $V_{o1}$  and taking partial derivatives with respect to process, the following is evaluated:

$$\Delta V_{o1} = \frac{\Delta V_{DD}}{A_1 + 1} + \Delta \text{----- (12)}$$

For large value of  $A_1$ , total variation of  $V_{o1}$  is given as

$$\Delta V_{o1} = \Delta V_{th} \text{----- (13)}$$

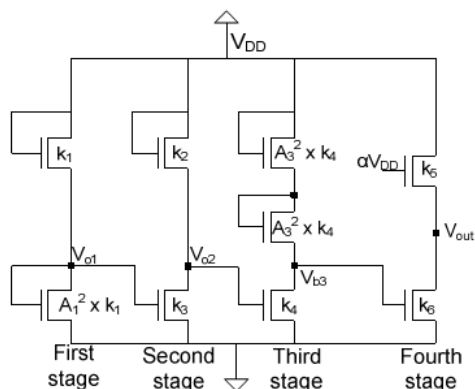


Fig3: biasing circuit design for tocounter the process variation in LNA

### B. Second Stage:

Applying KCL at node Vo2 and taking partial derivatives gives us the following expression:

$$\Delta V_{o2} = \Delta V_{DD} - \Delta I \quad \text{----- (14)}$$

### C. Third Stage:

The third and fourth stages will allow us some flexibility in choosing  $\gamma$  to satisfy  $V_{out} = \gamma \Delta V_{th} + V_{gs1}$  and approximate the behavior in (11). The factor  $\gamma$  encompasses effects such as channel length modulation and short channel effects which are not taken into account in the idealized square law current equations. By applying KCL at node Vb3 and taking partial derivatives, we are able to obtain an expression which contains both coefficients of  $\Delta V_{DD}$  and  $\Delta V_{th}$ .

$$\Delta V_{b3} = \Delta V_{DD} \left( \frac{A_3 - 2}{A_3} \right) + \Delta V_{th} \left( \frac{4 - 2A_3}{A_3} \right) \quad \text{----- (15)}$$

These coefficients are controllable by sizing the third stage and, along with proper sizing of the transistors of the fourth stage, we can optimize the design of the bias circuit by picking the best value of  $\gamma$  which gives lowest variation min S21, but may not in fact exactly mirror (11).

### D. Fourth Stage:

The output of the fourth stage,  $V_{out}$ , is used to bias transistor M2 of the LNA. The analysis of this stage is similar to those of previous stages. For  $V_{out}$  to be supply independent, the following relation is established between the sizes of the transistors:

$$\sqrt{k_5} = \frac{\sqrt{k_6}}{\alpha} \left( \frac{A_3 - 2}{A_3} \right) \quad \text{----- (16)}$$

We can now use (15) and (16) to set the value for  $\gamma$ . A also assists in establishing the nominal dc voltage at the output. The expression for  $\gamma$ , based on circuit parameters, is shown in (17).

$$\gamma = \alpha \left( \frac{3A_3 - 4}{A_3 - 2} \right) - 1 \quad \text{----- (17)}$$

To solve above equation for  $\gamma$  and sizing of the fourth stage, values of  $\alpha$  and  $A_3$  were iteratively picked in simulations. Results confirmed that, when  $\alpha$  was set to 1, choosing  $A_3$  to 5 resulted in lowest variations in S21 of the LNA, while providing the desired nominal dc value at  $V_{out}$ .

## V. SIMULATION RESULTS

We ran Monte Carlo simulations including effects from wafer level variation and local device mismatch at room temperature in the Cadence Spectre simulator. Realcomponents are used for all circuit elements in the LNA other than the inductors. The LNA designed operates at a center frequency of 6.4GHz. The baseline case, which has both input transistors M1 and M2 connected to a constant external bias, has a mean S21 magnitude of 1.85 with a standard deviation of 0.162 which gives it a variation of 8.75% about its mean value at room temperature.

The compensated LNA, which has the dc value of M2 being provided by the bias circuit, has a mean S21 magnitude of 1.89 with a standard deviation of 0.024 giving it a variation of 1.27%. The bias circuit decreases the variation in S21 by 85%. Histograms for S21 of both the uncompensated and compensated LNA are shown in Fig.4. Histograms of the magnitude of S21 of the LNA (a) without compensation and (b) with compensation. The supply voltage was swept and the gain recorded for both the uncompensated and compensated LNA. As shown in Fig. 5, S21 for the uncompensated LNA changes by 16% from its mean value. S21 for the compensated system changes only by 2.5%.

To ensure that the compensation scheme would work under extreme conditions, process corner simulations were carried out over a temperature range of -500C to 1000C, as shown in Table I. For the uncompensated LNA, the worst case is the slow-slow corner at -500C, when the gain deviates from its mean value at room temperature by 55%. For the compensated LNA, under the same conditions, the maximum variation is 10%.

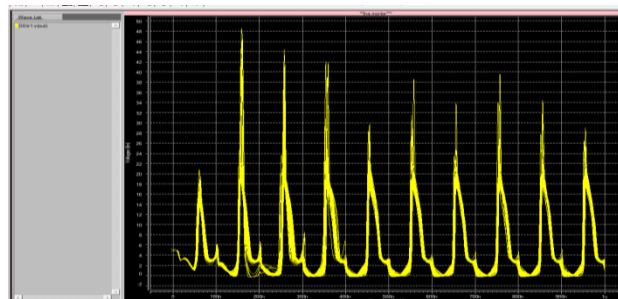


Fig4(a): simulation results for without compensation

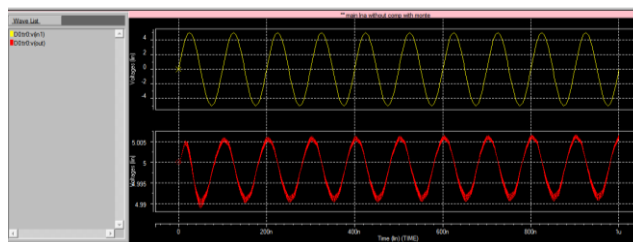


Fig4(b): simulation results for with compensation

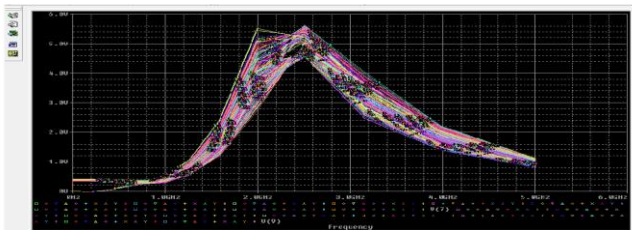


Fig4(c):monta carlo simulation of the gain and frequence of the LNA with out compensation

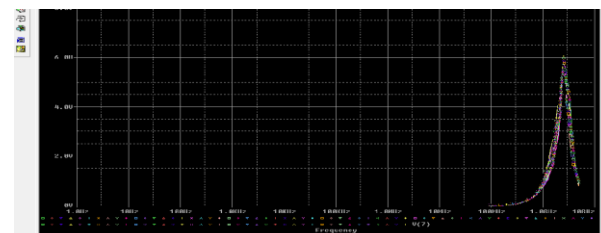


Fig4(d): monta carlo simulation of the gain and frequence of the LNA with out compensation

The bias circuit has a power overhead of 1.3mW and requires additional area of 588  $\mu\text{m}^2$ . The standalone LNA consumes 3.3mW. This additional cost in power and area is not excessive, considering the large reduction in variability of S21.

## VI. CONCLUSION

We have demonstrated a compensation scheme for low noise amplifiers in the 65nm process technology. Without any post fabrication trimming, the novel bias circuit scheme reduces variations in S21 due to manufacturing effects by 85%. The compensation scheme is robust under all process corners and a wide range of operating temperature. The technique can also very easily be ported to other RF amplifiers and significantly improve reliability with very little area and power overhead, translating to low cost and higher yield for RF systems.

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