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Modeling and Simulation of LDMOS Device

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Abstract: Laterally Diffused MOSFET (LDMOS) are widely used in modern communication industry and other applications. LDMOS offers various advantages over conventional MOSFETs with little process change. In the present paper, an LDMOS device is modeled and simulated in SILVACO device simulator package using the ATHENA and ATLAS modules. The complete fabrication process is modeled and the device performance is simulated. The modeled device gives a 46 V breakdown voltage for a device gate length of 5µm. The device threshold voltage is 0.97V. The device characteristic are also simulated and presented.

***Index Terms*—LDMOS, SILVACO, ATHENA, ATLAS**

I. INTRODUCTION

Aparadigm shift from thick and rigid electronic chips to flexible ultra thin chips has resulted in an entire new realm of electronic applications. 3D ICs, flexible circuits, RFIDs are a few of the numerous applications. The flexible circuits require mechanically rugged flexible substrates, ultra thin substrates and low cost production. Handling of ultra-thin chips is a major issue in flexible electronics circuits. The conventional methods of backside CMP are not efficient beyond 50µm thickness. Chipfilm^{TM} technology provides a non-conventional technique of obtaining ultra thin substrates. Before fabrication, the conventional bulk silicon wafers are processed through Chipfilm^{TM} technology.

Integration of organic, amorphous Silicon and poly-Silicon transistors on flexible substrates was presented by Bock [1] and Troccoli [2]. Crystalline silicon transistors better suited for efficient systems cannot be directly fabricated on flexible substrates. Li et al. [3] proposed a method to transfer the pre-fabricated thin film single crystal silicon transistors on flexible substrates.

LDMOS is a mature technology with its long usage in the wireless industry and has an excellent reliability record [4]. The main driver for LDMOS is a high volume application, which enables continuous improvement of the LDMOS technology [5], [6],. The device design of LDMOS enables high voltage withstanding capability through the drift regions [7]. RESURF technique presented in [8] further enhances the breakdown voltage level. LDMOS is projected as a technology of choice for high power applications as compared to GaAs, GaN [9]. LDMOS process is compatible with the BCD technology [10]. A method of fabricating LDMOS device was given by Smayling and Torenno [11]. Mosher [12] fabricated and demonstrated a self aligned RESURF region LDMOS device. Medium voltage LDMOS device was fabricated by Efland [13]. Formicon [14] presented a LDMOS device for 32V LDMOS technology with a power performance upto 130W in 2.7-3.5GHz frequency band with a 36% drain efficiency. A Si LDMOS power amplifier with 45% power efficiency was demonstrated in [15]. Ankarcrona [16] presented the modeling of RF LMDOS transistor with the effect of substrate on the output resistance of the device. Large signal analysis of the substrate effects on RF-SOI LDMOS transistors was carried out by Vestling [17]. Wagner [18] modeled the thermal effects in RF LDMOS transistors. A large signal Model for RF LDMOS Transistors was given by Tamoum [19]. The graded channel and quasi saturation effect in power LDMOS device were presented in [20]. Modeling and parameter extraction for LDMOS is detailed in [21].

In this paper, a single-crystalline silicon based LDMOS transistor design is presented on a Chipfilm^{TM} substrate. The device fabrication process is designed and simulated using a process simulator. Finally the device structure generated from the process simulator is analyzed for its performance using a device simulator package. The fabrication process is kept simplest and as similar to the standard CMOS device fabrication so that it is compatible and in lieu with the standard CMOS processes.

II. LDMOS BASICS

LDMOS transistors are voltage controlled devices, hence unlike the bipolar devices, there is no gate current flowing the gate. Hence the bias circuitry is very much simplified as compared to the bipolar devices. The majority of the LDMOS devices have the source connected to the backside of the device. Hence, the requirement of toxic BeO packages is eliminated. The bulk source can be eutectically soldered to the package and the bond wire requirement is removed reducing the inductance. The LDMOS devices show better temperature stability than the bipolar devices. Also they provide device stabilization preventing oscillations at higher frequencies. A cross section schematic of the LDMOS is shown in Fig. 1. The device has a sinker diffusion connecting the source to the backside substrate. The device consists of a drain extension which help realize higher breakdown voltages. The drain is shielded from the gate by metal field plate realizing extremely low feedback capacitance. The higher breakdown value in LDMOS is due to the Reduced Surface Field technology. In RESURF, one horizontal p^-n junction and a vertical p^+n junction develop two diode structures. The vertical diode shall have a lower breakdown voltage determined by the epitaxial doping level. The horizontal junction breakdown voltage is higher due to the high ohmic substrate. At thinner layers of the epitaxial layer, the depletion of the vertical junction becomes more and more reinforced by the horizontal junction. Hence for the same applied voltage, the depletion layer stretches along the surface longer than expected from one-dimensional

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01 June 2015

calculation. After a certain thickness, the reduced surface field does not reach the critical value even at high voltages and hence the breakdown is eliminated or raised to very high voltages.This forms the basis of an increased breakdown voltage LDMOS device.

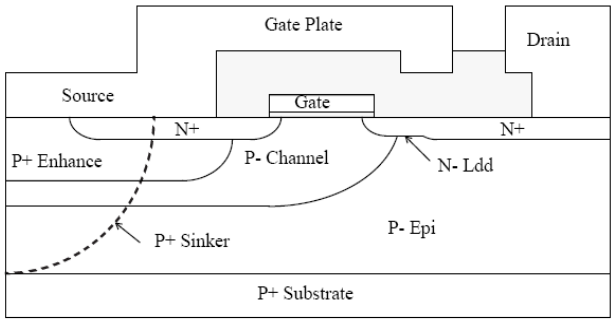

Fig. 1. Basic LDMOS device structure

III. LDMOS Fabrication Process

The LDMOS Fabrication process is presented in Table I. The process starts with a conventional bulk silicon wafer. In Chipfilm^{TM} technology 1-2µm thick wafer surface is the substrate. An epitaxial layer is grown over this layer. The buried p^+ doping profile of the Chipfilm^{TM} wafers is replicated in process simulator by simulating the epitaxial layer growth over a p^+ layer. A p-epitaxial layer of thickness 2µm is grown over the starting wafer. The epitaxial layer is p-doped with a boron concentration of 1×10^{15} cm^{-3}. A thin layer of gate oxide of thickness 57.3 nm is grown using dry oxidation process. A boron threshold voltage adjust implantation is carried out next. Next, the poly-silicon gate is deposited and patterned. Also, the region for drain extension diffusion is patterned and an n^+ implant is carried out to dope the poly-silicon gate and to produce a n-doped drain extension region besides the gate. The source and drain implant regions are patterned and n^+ implant is carried out. Finally a Fermi compress anneal followed by metal drain source contact deposition is carried out. The process parameters are detailed in Table II.

TABLE I
LDMOS Device Fabrication Process Steps

Step	Description
1	Starting material initial p-type substrate
2	p-epitaxy deposition
3	Gate oxide deposition by dry oxidation
4	Gate oxide patterning and polysilicon gate deposition
5	Poly silicon gate patterning
6	Patterning for drain extension diffusion
7	N^+ diffusion for poly gate and drain extension region
8	Source and drain region patterning
9	N^+ diffusion for source and drain regions
10	Fermi compress anneal
11	Contact electrode area patterning and metal deposition

IV. Process Modeling and Simulation

The LDMOS fabrication process is modeled and simulated in a process simulator tool. The device structure is simulated using the process simulator and a device simulator is used for the performance simulation. PEARSON model is used for ion implantation process as it is most suitable for asymmetrical implantation profiles. This function is used to obtain the longitudinal implantation profiles. The implantation profile as per the Pearson function is given by the differential equation:

$$\frac{df(x)}{dx} = \frac{(x-a)f(x)}{b_0 + b_1 x + b_2 x^2}$$

Mesh generation is an important step in the device and process simulation. In the present structure meshing of varying densities is used. The mesh density is finer near the junctions and also near the gate oxide. The coarse mesh is used in the substrate and the bulk epitaxy. This helps in getting accurate solutions without burdening the solver with large number of computing nodes. Fig 2 shows the meshing used for the LDMOS device under consideration.

TABLE II
Fabrication Process Parameters

Step	Description
Epitaxy deposition	Boron conc = 1e14, 45 min, 900ºC temperature
Dry oxidation	Duration 30 min, temperature 1000 ºC
V_t adjust implant	Boron implantation, dose = 6×10^{11}, Energy = 20keV
N^+ diffusion for poly gate and drain extension region	Phosphorous Dose = 2×10^{14}, Energy = 100keV
Source drain diffusion	Phosphorous Dose = 3×10^{15}, Energy = 100keV

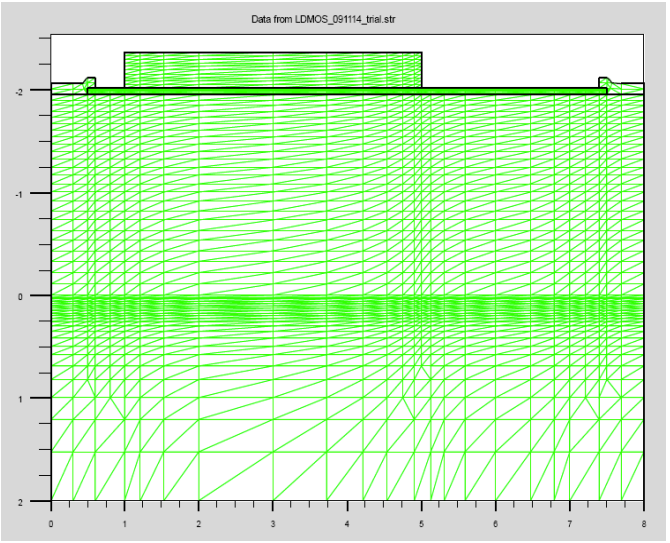

Fig. 2. Meshing for the LDMOS device structure

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01 June 2015

The intrinsic device is simulated without parasitic for DC and AC analysis. Drift-diffusion equations are solved to get the DC characteristics and the threshold voltage is extracted.

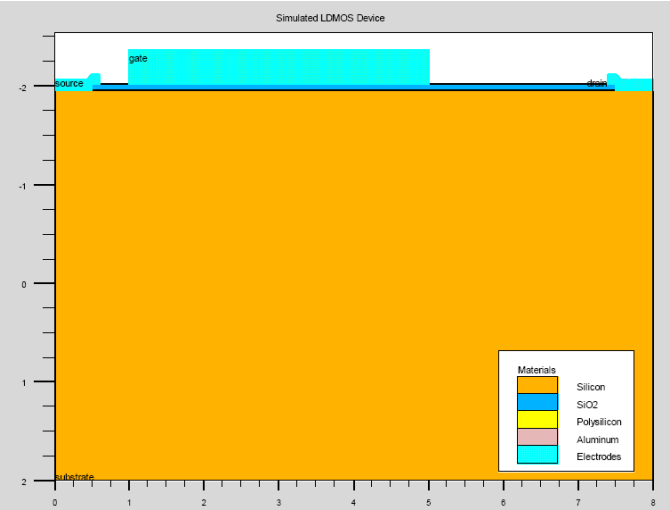

Fig.3. Simulated LDMOS Device

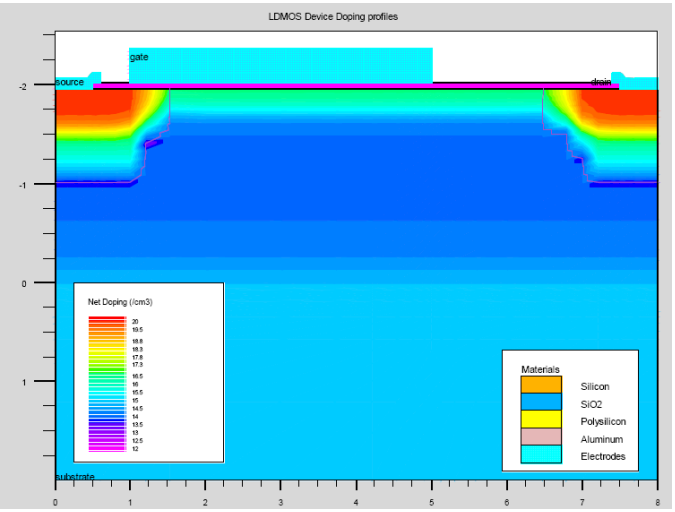

Fig. 4 Simulated LDMOS Device Doping Profile

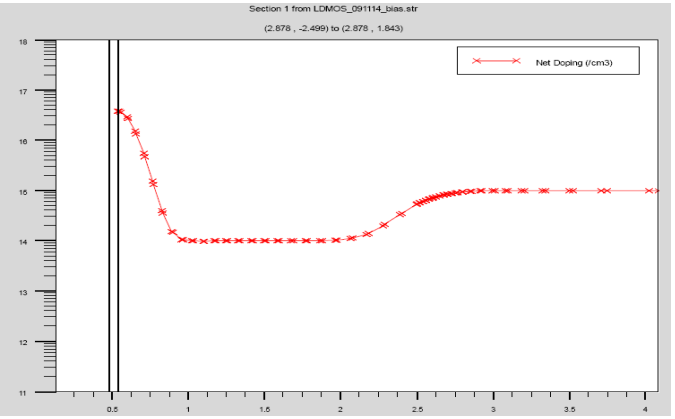

Fig. 5 Simulated LDMOS device net doping concentration

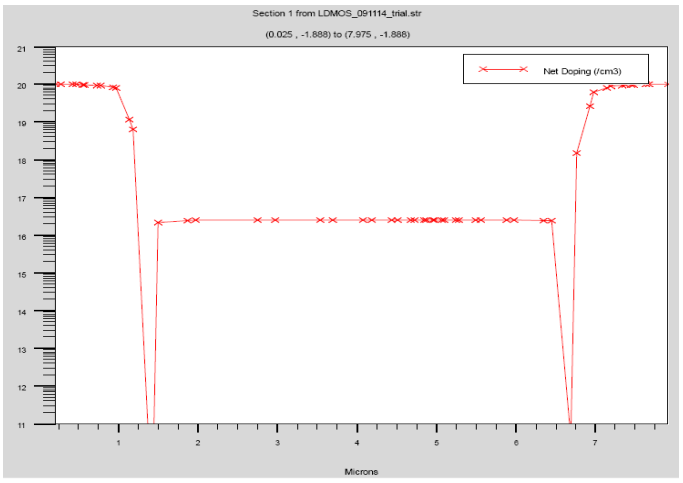

Fig. 6 Simulated LDMOS device net doping concentration along the channel

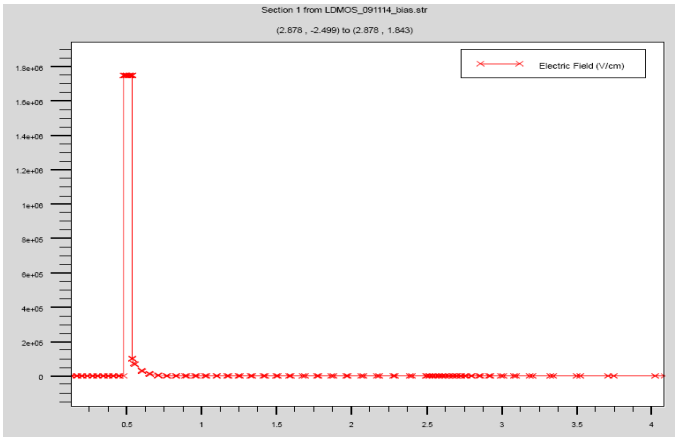

Fig. 7 Simulated Total Electric field

The extracted threshold value is in tune with the value obtained from the I_d-V_{gs} plot. The output characteristics of the device are also simulated. The device breakdown voltage is simulated by sweeping the drain voltage and observing the drain current.

V. Results and Discussion

A. General Device Characteristics

The simulated device structure is shown in Fig 3. Fig.4-6 gives the plot of doping profiles in the simulated device. Fig 7 presents the electric field distribution across the device. The electric filed is the highest near the interface between gate oxide and silicon where the channel is formed. The extracted oxide thickness for the dry oxidation process under conditions given in table II is 57.3nm.

B. DC Characteristics

The DC characteristics of LDMOS include the estimation

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01 June 2015

of the threshold voltage and the input output characteristics.

The threshold voltage extracted by device simulator is 0.97V. The I_d-V_{gs} plot of Fig 8 also shows a similar value of the threshold voltage.

The important characteristic of the LDMOS device is the high breakdown voltage. The device was simulated to extract the breakdown voltage by sweeping the drain source voltage. The device breakdown voltage is found to be 46 V. The plot of drain current with drain voltage swept up to breakdown is shown in Fig 9. The drain current shoots up instantly around 46V depicting an avalanche breakdown type phenomenon. The electric potential distribution from drain to source in the breakdown condition is shown in Fig 10. As seen from Fig 11, the electric field is maximum near the drain edge where the breakdown actually occurs and increases to a value near to the breakdown field of Si.

Device transconductance is derived from the AC analysis and is shown in Fig12.

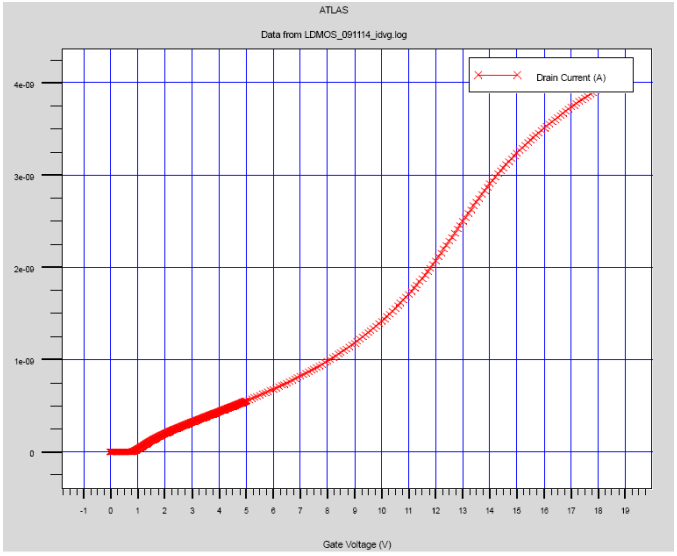

Fig.8 I_d-V_{gs} Plot

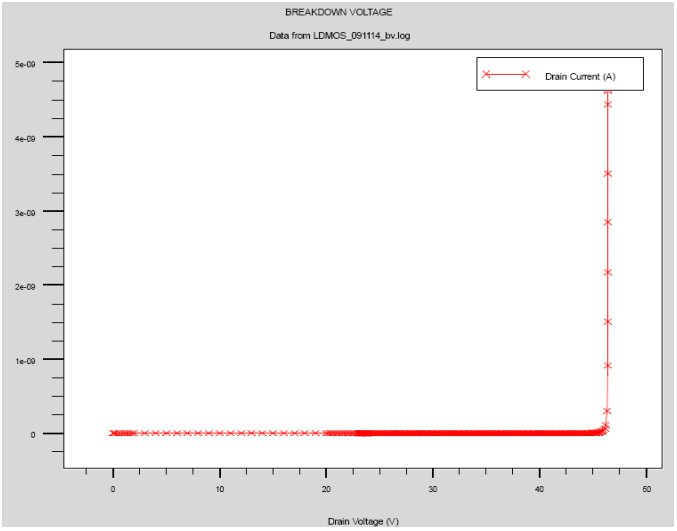

Fig.9. Simulated Breakdown Voltage Plot

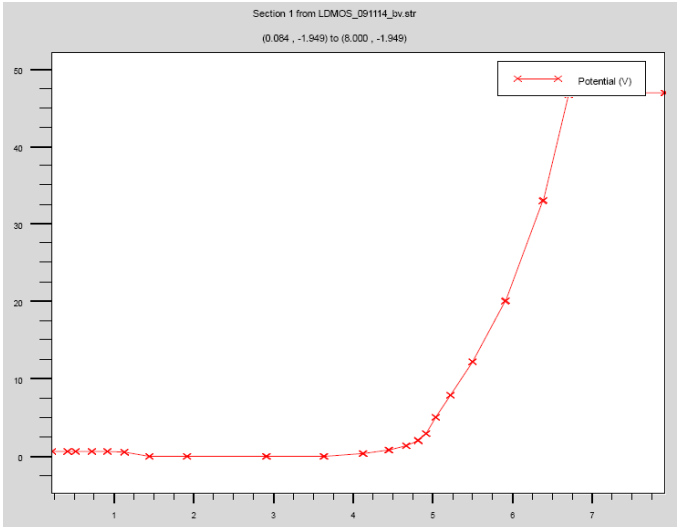

Fig.10. Electric Potential at Breakdown

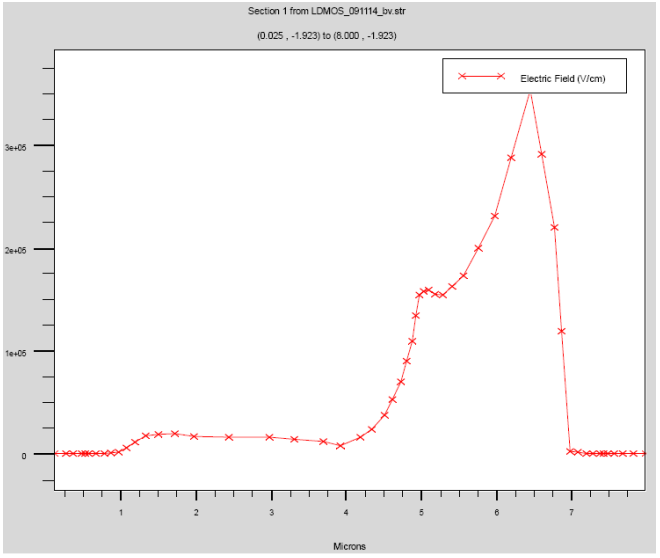

Fig. 11 Electric Field at breakdown

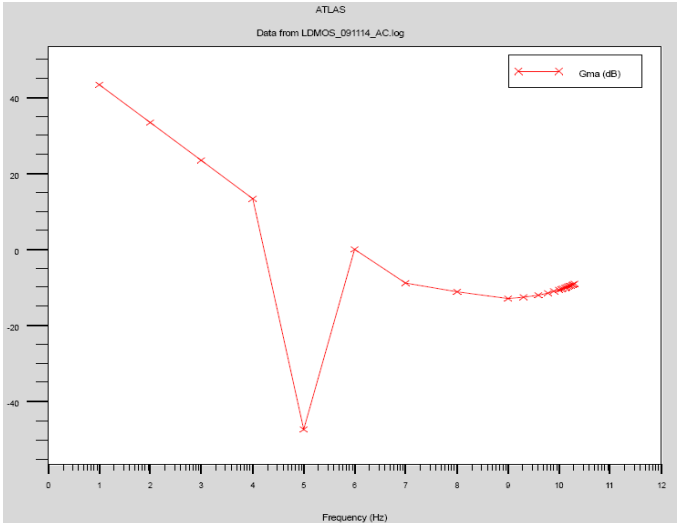

Fig.12. LDMOS transconductance plot

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01 June 2015

VI. CONCLUSION AND FUTURE WORK

The LDMOS process is modeled and the device structure is simulated for different operating characteristics.

The LDMOS device on ultra-thin substrates is a feasible structure and hence opens up numerous applications in the flexible electronic circuits. The process steps are also compatible with the standard CMOS fabrication sequence. Hence, the device fabrication can be carried out using the same process flow and along with the CMOS devices. High breakdown voltage LDMOS and CMOS devices can be fabricated on the same process.

The modeled device has an extended n-drift region between the gate and the drain. This region is responsible for enhancing the device breakdown voltage. The LDMOS device has a breakdown voltage of 46 V. The device demonstrates normal characteristics of a MOSFET device with a threshold voltage of 0.97V.

The device having demonstrated satisfactory characteristics is having large geometry. To device performance subject to the scaling down is an unexplored area which needs to be studied. The effect of scaling on the breakdown voltage and the device performance shall be taken up in the future.

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