International Journal of Engineering Research
Volume No.4, Issue No.6, pp : 303-308
ISSN:2319-6890)(online),2347-5013(print)
01 June 2015

Selective Harmonic Elimination PWM Technique Implementation for a Multilevel Converter

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Abstract:This paper presents the selective harmonic elimination technique implementation for hybrid seven-level cascaded multilevel converter. The converter configuration is the cascaded connection of a three-level Active neutral-point-clamped (ANPC) converter and an H-bridge per phase, thus forming a hybrid seven-level multilevel converter. The converter is operated by maintaining the switching frequency of a converter to a minimum value using selective harmonic elimination pulse width modulation (SHE-PWM). Analysis of the topology operated under SHE-PWM is presented on the basis of simulation results obtained from MATLAB/SIMULINK.

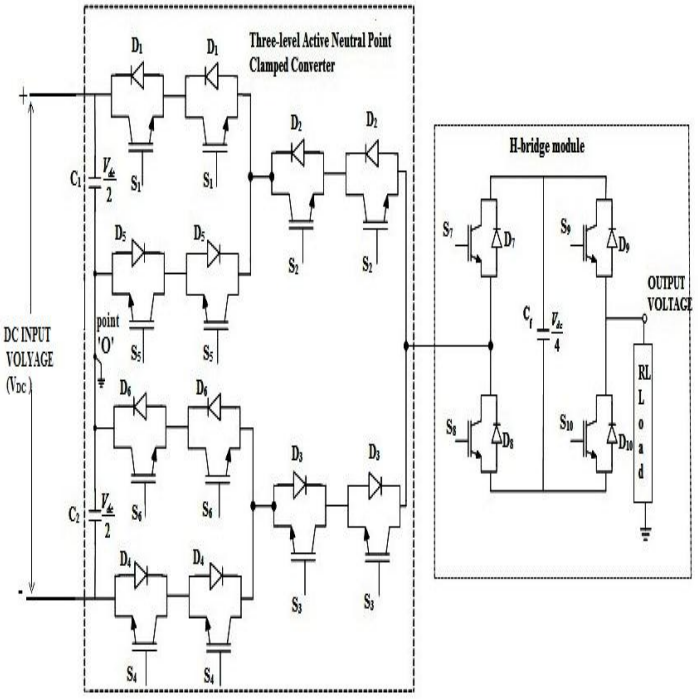
***Index Terms*—Multilevel converter, hybrid converter, Active neutral-point-clamped (ANPC) converter, hybrid converter, selective harmonic elimination pulse width modulation (SHE-PWM).**

INTRODUCTION

The Hybrid seven-level inverter presented in this paper is a cascaded connection of a three-level active neutral point clamped (ANPC) multilevel converter and an H-bridge per phase [1]. The three-level neutral-point clamped (NPC) based converters are the most widely used in industrial applications [2], but it deals with the unequal loss distribution among the semiconductor devices which confines the maximum output power and the switching frequency. To address this drawback active neutral-point clamped (ANPC) converter is employed which provides switching state redundancies in the zero-voltage level switching states. These properties make it very attractive topology in various industrial applications [3].

In order to extend the numbers of levels of the established multilevel inverters, and also to eliminate the need for individual DC sources for each converter stage, hybrid converter cascaded converter topologies with H-bridge cells have been used. The network configuration is based on the cascaded interconnection of a three-level inverter with an single H-bridge cell for each phase presented in [4 - 6]. For a given switching frequency, selective harmonic elimination PWM (SHE-PWM) offers the possibility of improved waveform quality compared to the existing modulation techniques (sinusoidal and space vector PWM). The three-level ANPC converter under SHE-PWM technique has been studied in [7], while the extension of this method to the five-level ANPC converter has presented in [8]. Hybrid multilevel converters are derived from various combinations of similar or different converter topologies.

The objective of this paper is to study the operation of a multilevel converter based on the series interconnection of a 3L-ANPC converter and individual H-bridges for each phase. The configuration of the circuit is shown in Fig. 1 [1].



Fig, 1.Circuit configuration of the Hybrid seven-level multilevel converter.

The operational principle of this hybrid seven-level ANPC-based multilevel converter is to analyze the voltage appearing across H-bridge capacitor under SHE-PWM. The limitations and effects in the voltage regulation of the floating capacitor of H-bridge for different loads and modulation indices are analyzed under SHE-PWM.

OPERATION OF THE CONVERTER

The cascaded interconnection of a ANPC-based multilevel converter and an H-bridge per phase shown in Fig.1.consists of two dc-link capacitors C_1 and C_2 which provides the midpoint voltage required for the 3L-ANPC converter. Due to the mid-point voltage, dc-link capacitor voltage is maintained to an average of V_{dc} /2 each. The voltage of H-bridge sub module capacitor (C_f) is maintained equal to V_{dc}/4 by considering a dc-link voltage of V_{dc}. The ANPC converter clamped to the neutral

ISSN:2319-6890)(online),2347-5013(print)
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point ensure the equal voltage sharing between the switches (S_1—S_4) and also create additional zero-voltage level switching states at point "O".

The hybrid converter presented in this paper is been operated to obtain 7 switching states as shown in Table I. These switching states generate the seven different voltage levels namely, $3V_{dc}$, $2V_{dc}$, V_{dc} , 0 , $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$. The switching states are the combination of the six switching states(S_1-S_6) of the 3L-ANPC converter and the four switching states(S_7-S_{10}) provided by the H-bridge submodule.

TABLE I

SWITCHING STATES OF THE SEVEN-LEVEL HYBRID ANPC-BASE MULTILEVEL CONVERTER

Voltage levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
0	0	0	0	0	0	0	0	0	0	0
V_{dc}	1	1	0	0	0	0	1	0	0	1
$2V_{dc}$	1	1	0	0	0	0	0	1	0	1
$3V_{dc}$	1	1	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0	0	0
$-V_{dc}$	0	0	1	1	0	0	0	1	1	0
$-2V_{dc}$	0	0	1	1	0	0	0	1	0	1
$-3V_{dc}$	0	0	1	1	0	0	1	0	0	1

The voltage control of the H-bridge capacitor to its reference voltage value of $V_{dc}/4$ is done through the switching states of the H-bridge submodule. Depending on the switching states to the H-bridge module, the floating capacitor (C_f) is either charged or discharged.

Since these voltage levels/states can be obtained by only one switching state and there is no redundant switching state, the change in the voltage across the floating capacitor (C_f) is determined only by the direction of the output phase current.

IMPLEMENTATION OF SHE-PWM

A multilevel selective harmonic elimination pulse width modulation (SHE-PWM) is an off-line (pre-calculated) non carrier based PWM technique. In this method the basic square-wave output is "chopped" a number of times, which are obtained by proper off-line calculations. Fig. 2. shows a generalized quarter-wave symmetric stepped voltage waveform synthesized by a (2m+1) -level inverter, where 'm' is the number of switching angles [9].

By applying Fourier series analysis, the amplitude of any odd n^{th} harmonic of the stepped waveform can be expressed as below expression, whereas the amplitudes of all even harmonics are zero.

$$h_n = \frac{4}{n\pi}\sum_{k}^{m}[V_k \cos(n\alpha_k)] \qquad (1)$$

Where V_k is the K^{th} level of dc voltage, n is an odd harmonic order, m is the number of switching angles, and a_k is the mth switching angle.

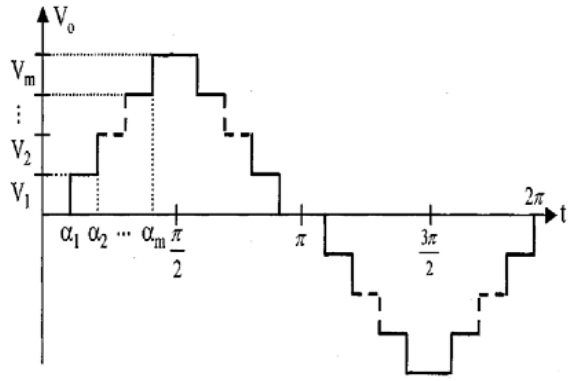

Fig.2. Generalized stepped voltage waveform.

The formulation of the SHE-PWM problem and acquisition of the solutions for seven-level waveform has been studied in [9]. The above equation can be further expressed as (2) for the fundamental frequency component and in (3) for the higher order harmonics

$$\sum_{i=1}^{N1}(-1)^{i+1}\cos(\alpha_i)+\sum_{i=N1+1}^{N1+N2}(-1)^{i}\cos(\alpha_i)+\sum_{i=N1+N2+1}^{N}(-1)^{i+1}\cos(\alpha_i)=M \qquad (2)$$

$$\sum_{i=1}^{N1}(-1)^{i+1}\cos(n\alpha_i)+\sum_{i=N1+1}^{N1+N2}(-1)^{i}\cos(n\alpha_i)+\sum_{i=N1+N2+1}^{N}(-1)^{i+1}\cos(n\alpha_i)=0 \qquad (3)$$

Where N_1 is the number of switching between the zero and the first level, N_2 is the number of switching between the first and the second levels, N_3 is the number of switching between the second and the third levels in the quarter period of the waveform, M is the modulation index, and α_i is the i^{th} switching within the quarter period of the waveform. The additional restriction imposed is

$$0 \le M \le 3 \qquad (4)$$

and

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \ldots\ldots < \alpha_N < \pi/2 \qquad (5)$$

and the amplitude of the fundamental component is

$$\widehat{V_1} = \frac{4.M}{\pi}V_{dc}$$

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to m-1 harmonic contents can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits. To keep the number of eliminated harmonics at a constant level, all switching angles must be less than π/2.

ISSN:2319-6890)(online),2347-5013(print)
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SWITCHING ANGES CALCULATION

Here the analysis for the switching angles is done using the equations (2) and (3). For total number of Switching angles (N) as five and keeping Modulation Index(M) as one, from expression(2) and (3),we get

$\alpha_1 = 20.3455^0$
$\alpha_2 = 31.1286^0$
$\alpha_3 = 41.5084^0$
$\alpha_4 = 61.5168^0$
$\alpha_5 = 64.4158^0$

Where N is the number of switching angles,
M is the modulation index.

α_1 , α_2 , α_3, α_4, α_5 corresponds to firing angles for all the switches in the H-bridge submodule. The firing angles for 3L-ANPC converter are the pulses obtained from the comparison of sine wave and saw tooth wave depending on the amplitude on the sine wave keeping saw tooth wave at constant amplitude.

An important property of the SHE-PWM technique is the existence of multiple solutions due to the non-linear and transcendental nature of the equations describing the problem. For multilevel waveforms the range of these multiple solutions depends upon the way the problem is formulated [11], the number of levels and the number of angles distributed on each level. This property has been presented in Fig. 3. which shows the graph between Switching angles (deg) and Modulation index(M). It can be observed that for the same modulation index a number of solutions for different angles distribution can be found.

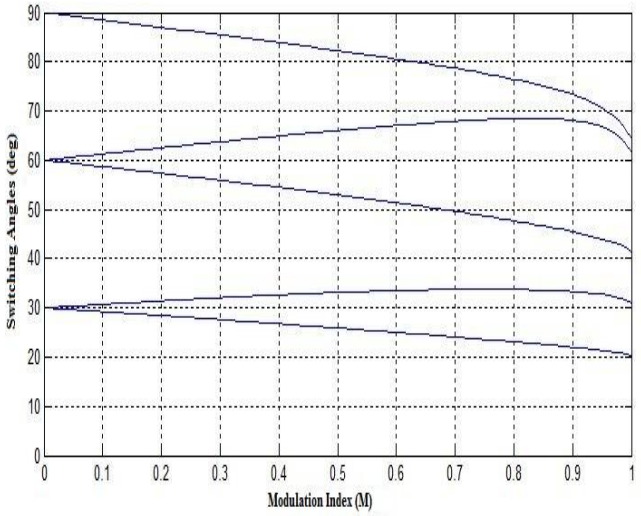

Fig.3. SHE-PWM solution trajectories.

I. GATING SIGNALS AND SWITCHING FREQUENCY GENERATION

(i). Generation of gate pulses for the 3L- ANPC converter

The simplest way of generating a fixed frequency pulse width modulated (PWM) signal is by comparison of sine wave with a linear slope waveform such as sawtooth wave as shown in Fig.4. The output signal goes high when the sine wave is higher than the sawtooth. When one input is greater than the other the output of the comparator goes to logic high. The output of the comparator gives gating signals/pulses applied to the switches of the three level ANPC converter that turns them ON for a fixed period time. These gate signal is applied to each switches S_1 to S_6 of ANPC converter.

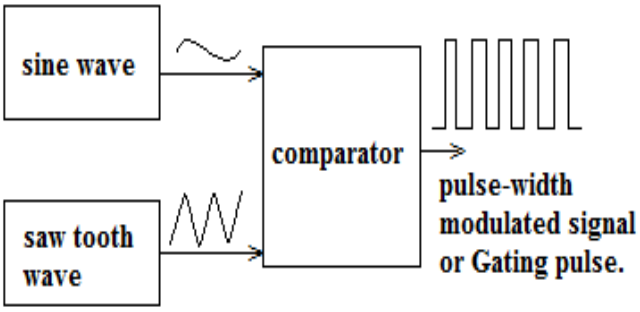

Fig.4. Generation of gating signals for 3L- ANPC converter switches.

submodule is done by first comparing the sine wave and linear slope saw tooth wave which results in a pulse-width modulated signal. This PWM signal is ANDed with switching pulses obtained from the comparison of different switching angles based on their values. The output of logical operator that gives gate pulse is applied to the gate terminal of the H-bridge switch. The gate signal is applied to the switches S_7 to S_{10} in the H-bridge submodule.

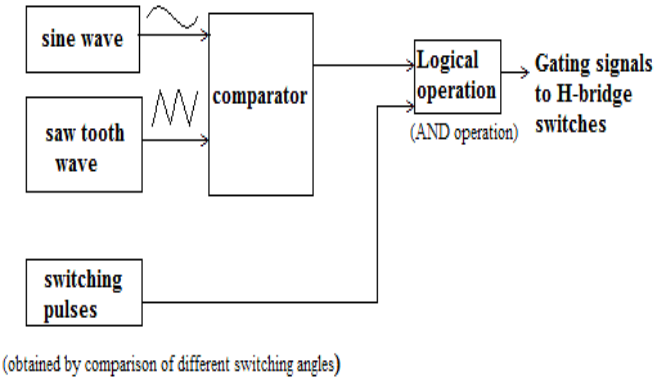

Fig.5. Generation of gating signals for H-bridge switches.

For a given operating point or converters operating within a limited range of modulation index and loads, solution patterns that provide curves with larger total charge are preferable, as the floating capacitor voltage can be controlled.

II. SIMULATION DIAGRAM AND RESULTS

The hybrid seven-level cascaded multilevel converter under SHE-PWM is simulated in MATLAB/SIMULINK for the parameters shown in Table II.

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TABLE II
Simulation parameters

DC link Voltage	400V
Flying capacitor (C_f)	1000µF
DC- link Capacitor (C_1 = C_2)	3300µF
Load A	R = 30Ω ; L = 40mH
Load B	R = 12Ω ; L = 35mH
Load C	R = 60Ω ; L = 120mH

Simulated circuit in MATLAB/SIMULINK as per the circuit configuration in Fig. 1. Is shown in Fig. 6.

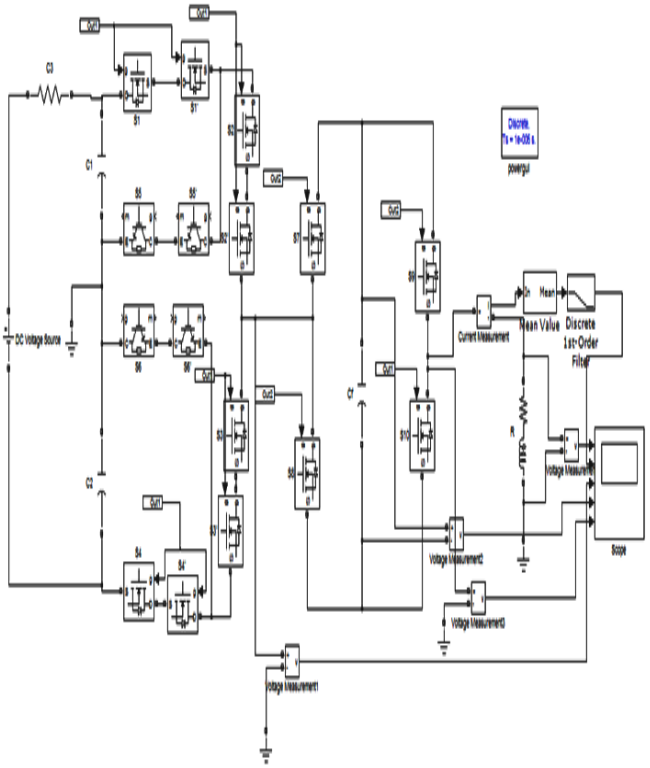

Fig. 6. Simulation diagram of the Hybrid seven-level cascaded ANPC based multilevel converter

The simulation results for a Modulation index of M=1 and number of switching angles N=5 for Load A are shown in Fig. 7. Fig. 7(a) shows the output phase voltage, Fig. 7(b) shows the output phase current, while Fig. 7(c) and (d) shows the voltages of the 3L-ANPC output voltage and H-bridge capacitor voltage. Fig. 7(e) shows the H-bridge output voltage.
The Total harmonic distortion obtained from the FFT analysis of output voltage shows the elimination of 3rd , 5th , 7th and 9th harmonics in table III.

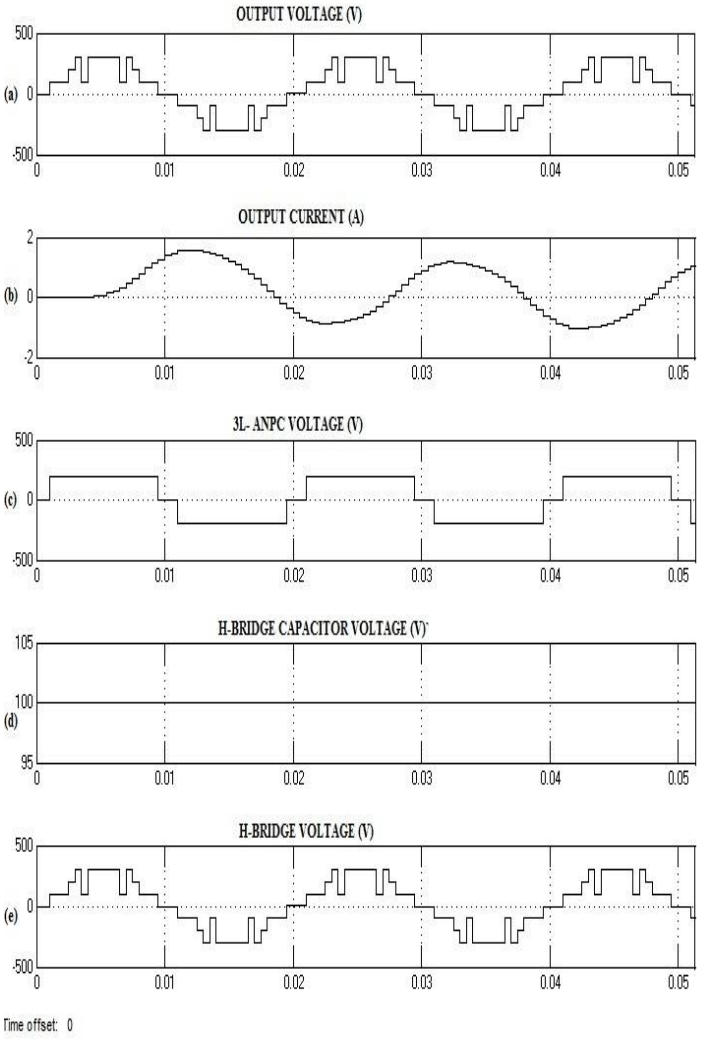

Fig.7. Simulation results for N=5 and M=1 for Load A. (a) Output phase voltage. (b) Output phase current. (c) 3L-ANPC voltage. (d) H-bridge capacitor voltage. (e) H-bridge voltage.
In the above graph it can be observed, the output phase voltage has the maximum value of 300V and minimum value of -300V. The output phase current increases to a maximum of 1.8A in the positive region, while the current decreases to a value of -1.6A in the negative region. In the 3L-ANPC converter voltage waveform the maximum voltage is 200V while the minimum voltage is -200V. The capacitor voltage of the H-bridge sub-module continuously charges and discharges to voltage of 100V depending on the switching pulses given to the H-bridge switches. The H-bridge output voltage is also shown which increases to voltage of 300V and decreases to -300V.

The THD values of 3rd, 5th , 7th and 9th harmonics Shown in table III are obtained from the FFT analysis of output voltage where the THD values equal to zero which signifies that the lower odd harmonics are eliminated.

ISSN:2319-6890)(online),2347-5013(print)
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Table III. THD values for Load A

ODD HARMONICS	THD (%)
3rd harmonic	0.01%
5th harmonic	0.00%
7th harmonic	0.01%
9th harmonic	0.01%

Similarly the output waveforms obtained for Load B and Load C have been shown in Fig. 8 and Fig. 9. .Table IV and Table V shows THD for 3rd, 5th, 7th and 9th harmonics for load B and load C respectively.

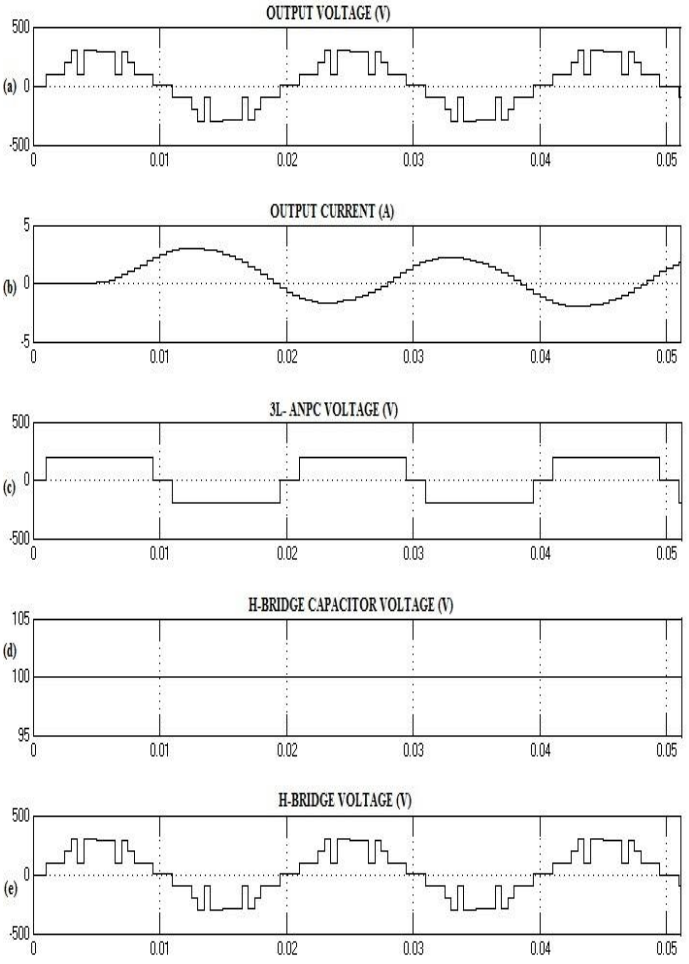

Fig.8. Simulation results for N=5 and M=1 for Load B. (a) Output phase voltage. (b) Output phase current. (c) 3L-ANPC voltage. (d) H-bridge capacitor voltage. (e) H-bridge voltage.

In the graph shown in Fig.8. it can be observed that the output phase voltage has the maximum voltage of 300V and a minimum voltage of -300V. The output phase current is of 3.2A, while the 3L-ANPC converter's voltage of ± 200V. The H-bridge capacitor voltage is maintained at 100V which charges and discharges depending on the switching pulses given to the H-bridge switches. The H-bridge submodule voltage has a voltage of ± 300V.

Table IV. THD values for Load B.

ODD HARMONICS	THD (%)
3rd harmonic	0.01%
5th harmonic	0.00%
7th harmonic	0.02%
9th harmonic	0.01%

The THD values obtained from FFT analysis of output voltage shows that the lower odd harmonics are nearly eliminated. The 5th harmonic is fully eliminated whereas remaining odd harmonics are nearly eliminated.

The output waveform shown in Fig .9 has a output voltage of ± 300V. Whereas the output phase current's peak value is 1.7A, the 3l- ANPC converter output voltage is ± 200V. The H-bridge capacitor is maintained at 100V which charges and discharges according to the switching pulses given to the H-bridge. The H-bridge voltage is ± 300V.

Table V. THD values for Load C.

ODD HARMONICS	THD (%)
3rd harmonic	0.02%
5th harmonic	0.00%
7th harmonic	0.01%
9th harmonic	0.01%

ISSN:2319-6890)(online),2347-5013(print)
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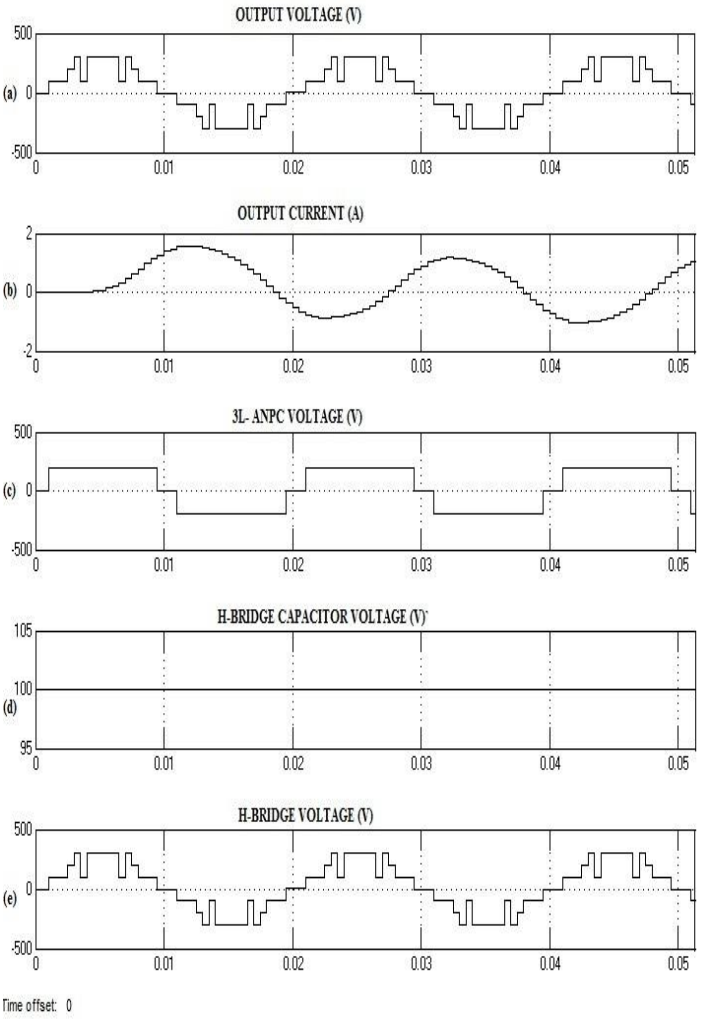

Fig. 9. Simulation results for N=5 and M=1 for Load C. (a) Output phase voltage. (b) Output phase current. (c) 3L-ANPC voltage. (d) H-bridge capacitor voltage. (e) H-bridge voltage.

The THD values obtained from the FFT analysis of output voltage shown in the above table presents that the lower odd harmonics 3^{rd} , 5^{th} , 7^{th} and 9^{th} are nearly eliminated.

III. CONCLUSION

For different values of loads, various output waveforms (viz. output voltage, output phase current, 3L-ANPC output voltage, H-bridge capacitor voltage and H-bridge voltage) has been presented along with the respective THD value. It is inferred that by keeping the switching frequency to power frequency, elimination of lower order harmonics can be obtained successfully by using the presented SHE-PWM technique. The performance of proposed configuration under SHE-PWM can also be validated experimentally. The same technique can be utilized for converter with similar range of dc-link voltages. The voltage of floating capacitor (C_f) has been regulated to obtain seven different voltage levels. A different value of loads has been chosen to show the versatility of chosen SHE-PWM technique.

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