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Optimized FIR Filter using Distributed Arithmetic Architecture

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Abstract : FIR filters are digital filters with impulse response of finite duration, because it settles to zero in finite time. They are also known as non-recursive filter because they do not have the feedback part. FIR filters can be used to design almost any type of frequency response in digital form and can be implemented using adders, multipliers and delay elements. Various architectures can be used for implementing FIR filters, one such is the Distributed Arithmetic. This is a multiplier less architecture, since multipliers are the speed limiting elements in a VLSI circuit. Thus it consumes less area than normal FIR filter by replacing multipliers with shift and add operation. In this paper an FIR filter is designed using Distributed Arithmetic in Xilinx ISE 14.7 by programming in VHDL.
Keywords : FIR filter, Distributed Arithmetic, multiplier less, shift and add, DSP.

I. Introduction

Signal is a function of independent variable that contains information. Signal processing is a method to extract information from a signal. There is Analog Signal Processing and Digital Signal Processing. Analog Signal Processing has both input and output as continuous signals and in Digital Signal Processing, input and output are discrete signals. Digital Signal Processing (DSP) finds applications in almost all walks of life. In Signal Processing, we need to remove noise from signals. A filter is a frequency selective network, which modify an input signal in order to facilitate further processing. In Signal Processing, filter is a device or an algorithm which removes parts of a signal. It selects, suppresses or modifies certain frequency components of the signal, either to reduce noise or to shape the spectrum. There are two types of filters, Analog filter and Digital filter. Analog filter operates on voltages whereas digital filter operates on numbers or discrete signals. Digital filters have better Signal to Noise Ratio, better reproducibility, and performs noiseless mathematical operations. Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter are two common types of digital filters. FIR is non recursive in nature and IIR is recursive in nature. FIR filter is a filter whose impulse response or the response to any finite length input, is of finite duration, because it settles to zero in finite time. IIR filters have internal feedback and may continue to respond indefinitely. FIR filter can be used to implement almost any sort of frequency response digitally and is implemented with multipliers, adders and delay elements.

II. Related Work

Digital Signal Processing (DSP) has a wide range of application. In digital signal processing, Digital filters are the important elements. They are widely used in multimedia audio signal processing in which noise is removed from audio signals. Designing digital filter is the process of calculating appropriate filter coefficients and order of digital filter. Digital Filters are of two types namely Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Due to its stability, FIR filters are preferably used. The basic representation of an FIR filter is given by (Eq. 1).

$$y(n) = \sum_{k=0}^{M-1} h_k\, x(n-k) \qquad (1)$$

Where y(n) is the output response, x(n) is the input signal and h_k represents the filter coefficients for the M tap FIR filter. M is the order of the filter. The direct form realization of an M-tap FIR filter is shown in Fig. 1.

In direct form representation, FIR filter can be realized using adders, multipliers and delay elements. But multipliers are the speed limiting elements in the circuit. Thus we can replace multipliers with shift and add operation, that is MCM (Multiple Constant Multiplication) in which a set of constants (here h_0, h_1,… is multiplied with a variable (here x(n)). But the disadvantage in shift and add method is that the

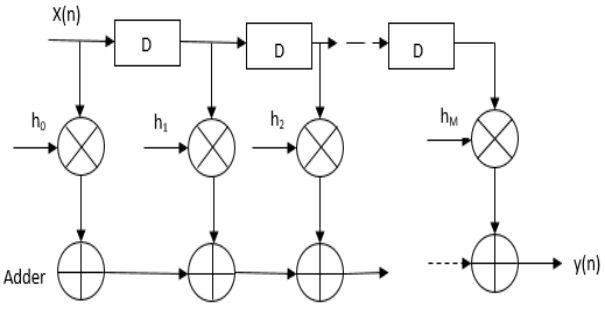

Fig. 1. Direct form representation of M-tap FIR filter

complexity and resource utilization is more. Another method is the use of transpose based structure. By using the transpose based architecture, switching activity at one or both inputs of the multipliers can be reduced. But the problem is that it requires more processing and memory. Pipelining is one other method in which multiple instructions are overlapped in execution thus accelerating the program execution time by increasing the number of instructions finished per cycle. But it creates an

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increase in circuit complexity and the performance is hard to predict. Thus we come to another architecture called Distributed Arithmetic (DA), is a multiplier less architecture. DA uses Look Up Tables (LUTs), delays and scaling accumulators to implement an FIR filter efficiently. Thus it increases speed of filtering process and consumes less area and hence it saves resources.

III. Proposed Work

Distributed Arithmetic (DA) is used for the calculation of inner product or multiply and accumulate (MAC) efficiently. It is the bit level rearrangement of the multiply and accumulate operation. This technique is bit serial in nature. DA is appropriate when the number of elements in a vector is almost same as the word size. In DA, ROM look-ups can replace the explicit process of multiplication. Thus we can efficiently implement an FIR filter on Field Programmable Gate Array (FPGA). The Fig. 2 shows the basic block diagram for FIR filter structure using Distributed Arithmetic.

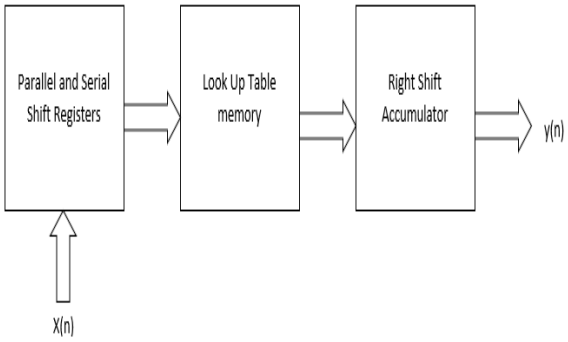

Fig. 2. FIR filter structure using Distributed Arithmetic

It includes mainly three blocks- Parallel and Serial Shift Registers, Look up table memory and right shift accumulator. Here x(n) is the input signal and y(n) is the output response.
The output response of linear, time-invariant filter at any discrete time is given by Eq.2.

$$y = \sum_{k=1}^{K} A_k \, X_k \qquad (2)$$

Let X_k be N-bits scaled 2's complement number and X_k:{b_{k0} , b_{k1}, b_{k2}, ……, $b_{k(N-1)}$} where b_{k0} represents sign bit. Thus X_k can be expressed in Eq.3.

$$X_k = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \qquad (3)$$

Substituting Eq.3 in Eq.2 and solving it completely, we get the output response as in Eq.4.

$$y = -\sum_{k=1}^{K} A_k \,.\,(b_{k0}) + \sum_{n=1}^{N-1} [\sum_{k=1}^{K} A_k \,.\, b_{kn}] 2^{-n} \qquad (4)$$

Table 1 shows a basic Look Up Table (LUT) for Distributed Arithmetic using 3 coefficients A_0, A_1, A_2. Based on the shift register output values, corresponding value is selected from the look up table memory.

IV. Results

An FIR filter is designed and synthesized using Distributed Arithmetic in Xilinx ISE 14.7 Design Suite and the programming is done in VHDL for a Spartan 3E-1200 FPGA as target device. The output waveform is shown in Fig. 3. Fig.4 and Fig.5 shows the RTL schematic and layout for the FIR filter using Distributed Arithmetic architecture.

Table 1. Look up table for 3 coefficients

$b_2b_1b_0$	Data
000	0
001	A_0
010	A_1
011	A_1+A_0
100	A_2
101	A_2+A_0
110	A_2+A_1
111	$A_2+A_1+A_0$

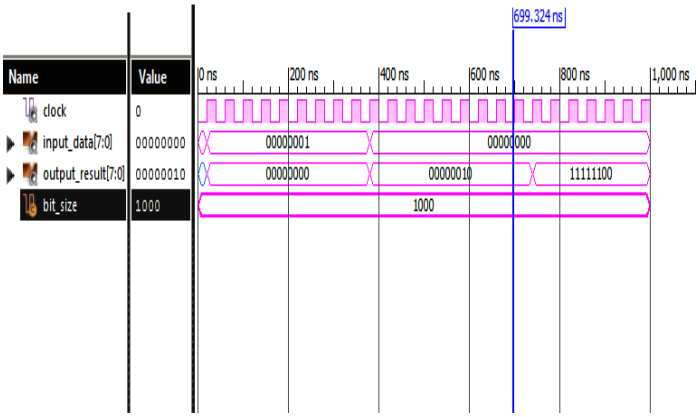

Fig. 3. Output waveform of FIR filter using DA

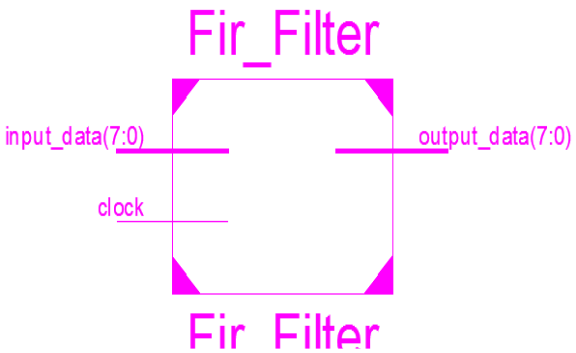

Fig. 4. RTL schematic of FIR filter using DA

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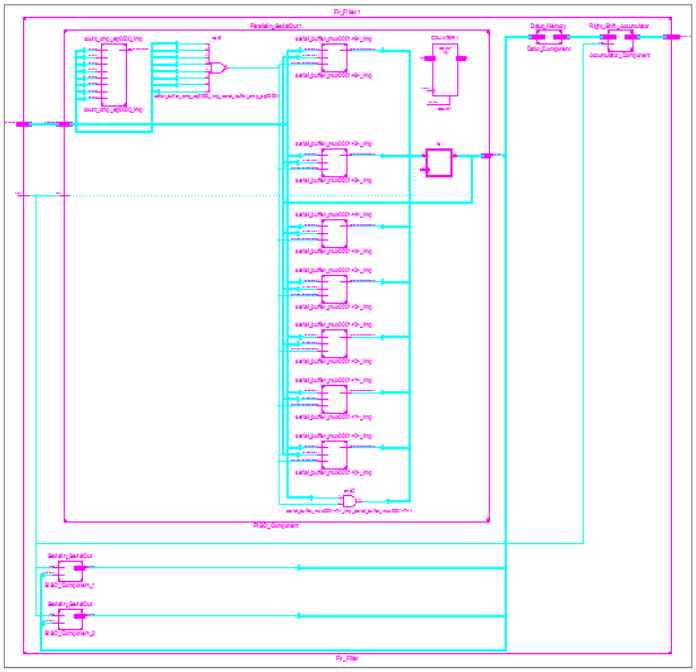

Fig. 5. Layout of FIR filter using DA

V. Conclusion

An FIR filter is designed using distributed arithmetic architecture in this paper. This is a multiplier less architecture. It uses look up tables, shift registers and scaling accumulators and thus consumes less resources. Distributed Arithmetic architecture can be thus used for high speed implementation of FIR filter. Since the Distributed Arithmetic architecture is basically bit serial in nature, as a future enhancement, we can further increase the speed by using a distributed parallel architecture.

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